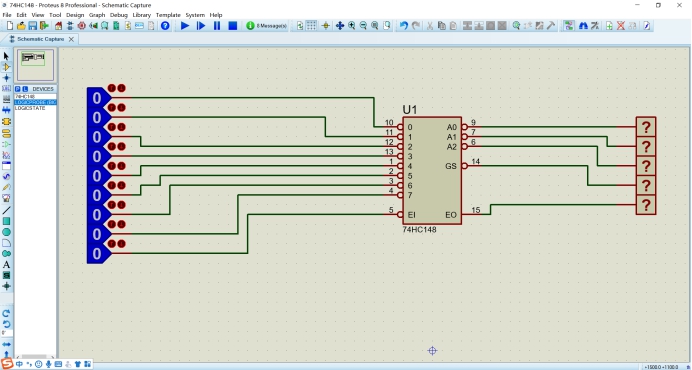
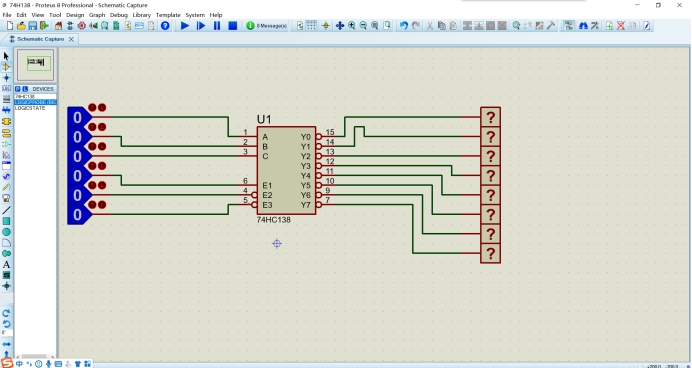
# 实验二实验结论

1. Protues电路图

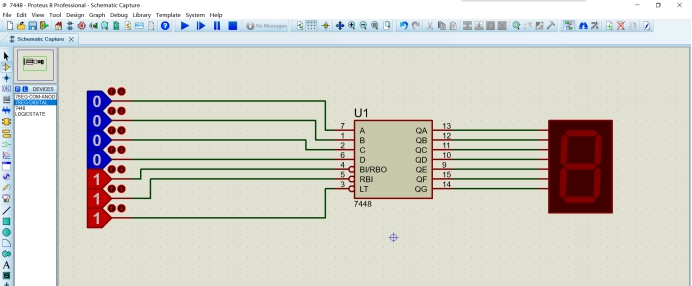
（1）8线-3线优先编码器



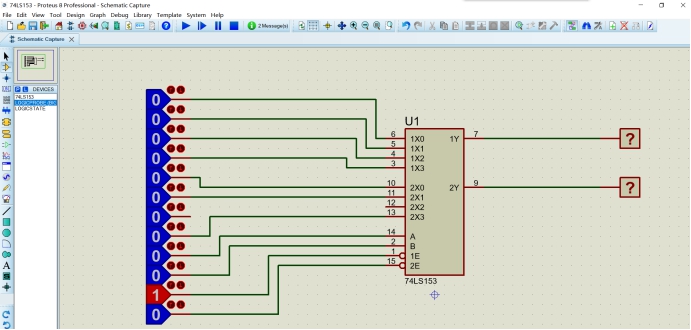
（2）3线-8线译码器



1. 显示译码器

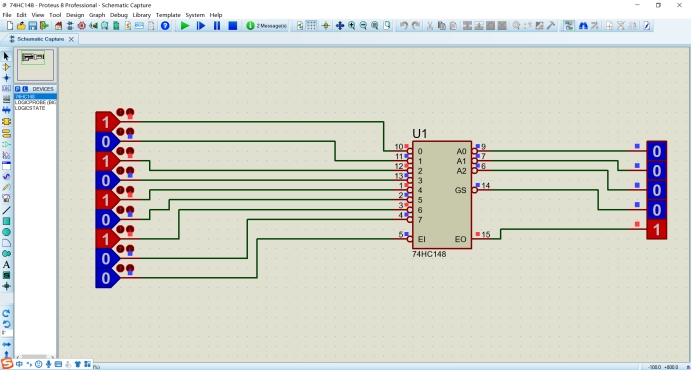


（4）多路选择器

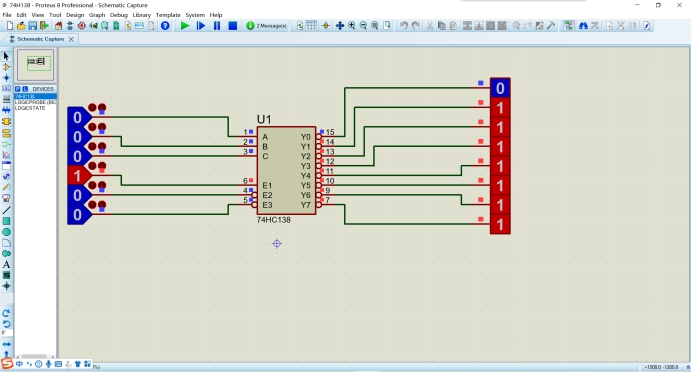


1. Protues仿真效果图

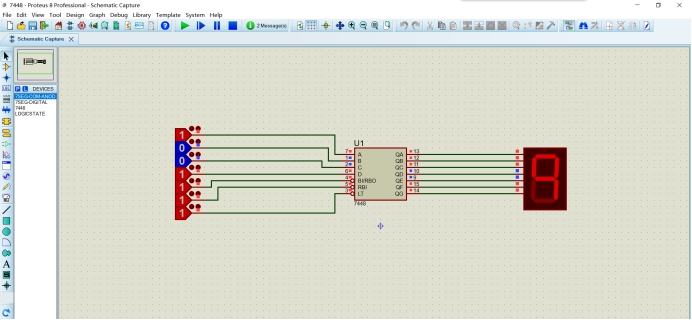
（1）8线-3线优先编码器



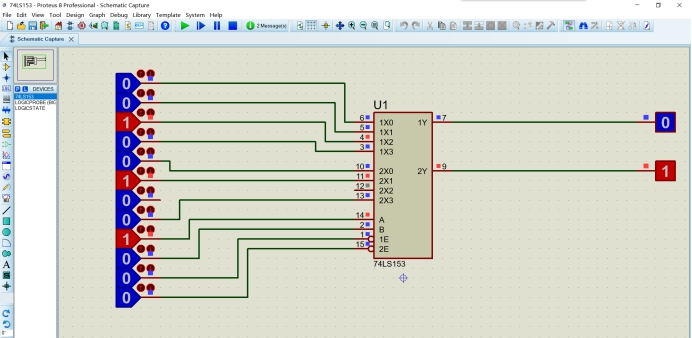
（2）3线-8线译码器



1. 显示译码器



（4）多路选择器



1. Quartus顶层文件原理图

（1）8线-3线优先编码器

module logic2(enb,a0,a1,a2,a3,a4,a5,a6,a7,dout0,dout1,dout2);

input enb,a0,a1,a2,a3,a4,a5,a6,a7;

output reg dout0,dout1,dout2;

always @ (enb,a0,a1,a2,a3,a4,a5,a6,a7)

if (enb==0)

begin

casex({a0,a1,a2,a3,a4,a5,a6,a7})

8'b11111111:begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 1;

end

8'b???????0:begin

dout0 <= 0;

dout1 <= 0;

dout2 <= 0;

end

8'b??????01:begin

dout0 <= 0;

dout1 <= 0;

dout2 <= 1;

end

8'b?????011:begin

dout0 <= 0;

dout1 <= 1;

dout2 <= 0;

end

8'b????0111:begin

dout0 <= 0;

dout1 <= 1;

dout2 <= 1;

end

8'b???01111:begin

dout0 <= 1;

dout1 <= 0;

dout2 <= 0;

end

8'b??011111:begin

dout0 <= 1;

dout1 <= 0;

dout2 <= 1;

end

8'b?0111111:begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 0;

end

8'b01111111:begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 1;

end

default :begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 1;

end

endcase

end

else

begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 1;

end

endmodule

（2）3线-8线译码器

module a74HC138(enb,a0,a1,a2,dout0,dout1,dout2,dout3,dout4,dout5,dout6,dout7);

input enb,a0,a1,a2;

output reg dout0,dout1,dout2,dout3,dout4,dout5,dout6,dout7;

always @ (enb,a0,a1,a2)

if (enb==0)

begin

casex({a0,a1,a2})

3'b111:begin

dout0 <= 0;

dout1 <= 1;

dout2 <= 1;

dout3 <= 1;

dout4 <= 1;

dout5 <= 1;

dout6 <= 1;

dout7 <= 1;

end

3'b110:begin

dout0 <= 1;

dout1 <= 0;

dout2 <= 1;

dout3 <= 1;

dout4 <= 1;

dout5 <= 1;

dout6 <= 1;

dout7 <= 1;

end

3'b101:begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 0;

dout3 <= 1;

dout4 <= 1;

dout5 <= 1;

dout6 <= 1;

dout7 <= 1;

end

3'b100:begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 1;

dout3 <= 0;

dout4 <= 1;

dout5 <= 1;

dout6 <= 1;

dout7 <= 1;

end

3'b011:begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 1;

dout3 <= 1;

dout4 <= 0;

dout5 <= 1;

dout6 <= 1;

dout7 <= 1;

end

3'b010:begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 1;

dout3 <= 1;

dout4 <= 1;

dout5 <= 0;

dout6 <= 1;

dout7 <= 1;

end

3'b001:begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 1;

dout3 <= 1;

dout4 <= 1;

dout5 <= 1;

dout6 <= 0;

dout7 <= 1;

end

3'b000:begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 1;

dout3 <= 1;

dout4 <= 1;

dout5 <= 1;

dout6 <= 1;

dout7 <= 0;

end

default :begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 1;

dout3 <= 1;

dout4 <= 1;

dout5 <= 1;

dout6 <= 1;

dout7 <= 1;

end

endcase

end

else

begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 1;

dout3 <= 1;

dout4 <= 1;

dout5 <= 1;

dout6 <= 1;

dout7 <= 1;

end

endmodule

（3）显示译码器

module a7448(enb,a0,a1,a2,a3,dout0,dout1,dout2,dout3,dout4,dout5,dout6);

input enb,a0,a1,a2,a3;

output reg dout0,dout1,dout2,dout3,dout4,dout5,dout6;

always @ (enb,a0,a1,a2,a3)

if (enb==0)

begin

casex({a0,a1,a2,a3})

4'b0000:begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 1;

dout3 <= 1;

dout4 <= 1;

dout5 <= 1;

dout6 <= 0;

end

4'b0001:begin

dout0 <= 0;

dout1 <= 1;

dout2 <= 1;

dout3 <= 0;

dout4 <= 0;

dout5 <= 0;

dout6 <= 0;

end

4'b0010:begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 0;

dout3 <= 1;

dout4 <= 1;

dout5 <= 0;

dout6 <= 1;

end

4'b0011:begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 1;

dout3 <= 1;

dout4 <= 0;

dout5 <= 0;

dout6 <= 1;

end

4'b0100:begin

dout0 <= 0;

dout1 <= 1;

dout2 <= 1;

dout3 <= 0;

dout4 <= 0;

dout5 <= 1;

dout6 <= 1;

end

4'b0101:begin

dout0 <= 1;

dout1 <= 0;

dout2 <= 1;

dout3 <= 1;

dout4 <= 0;

dout5 <= 1;

dout6 <= 1;

end

4'b0110:begin

dout0 <= 0;

dout1 <= 0;

dout2 <= 1;

dout3 <= 1;

dout4 <= 1;

dout5 <= 1;

dout6 <= 1;

end

4'b0111:begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 1;

dout3 <= 0;

dout4 <= 0;

dout5 <= 0;

dout6 <= 0;

end

4'b1000:begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 1;

dout3 <= 1;

dout4 <= 1;

dout5 <= 1;

dout6 <= 1;

end

4'b1001:begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 1;

dout3 <= 1;

dout4 <= 0;

dout5 <= 1;

dout6 <= 1;

end

4'b1010:begin

dout0 <= 0;

dout1 <= 0;

dout2 <= 0;

dout3 <= 1;

dout4 <= 1;

dout5 <= 0;

dout6 <= 1;

end

4'b1011:begin

dout0 <= 0;

dout1 <= 0;

dout2 <= 1;

dout3 <= 1;

dout4 <= 0;

dout5 <= 0;

dout6 <= 1;

end

4'b1100:begin

dout0 <= 0;

dout1 <= 1;

dout2 <= 0;

dout3 <= 0;

dout4 <= 0;

dout5 <= 1;

dout6 <= 1;

end

4'b1101:begin

dout0 <= 1;

dout1 <= 0;

dout2 <= 0;

dout3 <= 1;

dout4 <= 0;

dout5 <= 1;

dout6 <= 1;

end

4'b1110:begin

dout0 <= 0;

dout1 <= 0;

dout2 <= 0;

dout3 <= 1;

dout4 <= 1;

dout5 <= 1;

dout6 <= 1;

end

4'b1111:begin

dout0 <= 0;

dout1 <= 0;

dout2 <= 0;

dout3 <= 0;

dout4 <= 0;

dout5 <= 0;

dout6 <= 0;

end

default :begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 1;

dout3 <= 1;

dout4 <= 1;

dout5 <= 1;

dout6 <= 1;

end

endcase

end

else

begin

dout0 <= 1;

dout1 <= 1;

dout2 <= 1;

dout3 <= 1;

dout4 <= 1;

dout5 <= 1;

dout6 <= 1;

end

endmodule

（4）多路选择器

module mux41\_a(y,a0,a1,a2,a3,s1,s0);

output y;

input a0,a1,a2,a3;

input s1,s0;

reg y;

always @(s1 or s0 or a0 or a1 or a2 or a3)

begin

case({s1,s0})

2'b00: y = a0;

2'b01: y = a1;

2'b10: y = a2;

2'b11: y = a3;

default:y =1'bx;

endcase

end

endmodule

1. Quartus测试文件

（1）8线-3线优先编码器

// Copyright (C) 2018 Intel Corporation. All rights reserved.

// Your use of Intel Corporation's design tools, logic functions

// and other software and tools, and its AMPP partner logic

// functions, and any output files from any of the foregoing

// (including device programming or simulation files), and any

// associated documentation or information are expressly subject

// to the terms and conditions of the Intel Program License

// Subscription Agreement, the Intel Quartus Prime License Agreement,

// the Intel FPGA IP License Agreement, or other applicable license

// agreement, including, without limitation, that your use is for

// the sole purpose of programming logic devices manufactured by

// Intel and sold by Intel or its authorized distributors. Please

// refer to the applicable agreement for further details.

// \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// This file contains a Verilog test bench template that is freely editable to

// suit user's needs .Comments are provided in each section to help the user

// fill out necessary details.

// \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Generated on "03/04/2020 14:28:02"

// Verilog Test Bench template for design : logic2

//

// Simulation tool : ModelSim-Altera (Verilog)

//

**`timescale 1 ns/ 1 ps**

**module logic2\_vlg\_tst();**

**// constants**

**// general purpose registers**

**//reg eachvec;**

**// test vector input registers**

**reg a0;**

**reg a1;**

**reg a2;**

**reg a3;**

**reg a4;**

**reg a5;**

**reg a6;**

**reg a7;**

**reg enb;**

**// wires**

**wire dout0;**

**wire dout1;**

**wire dout2;**

**// assign statements (if any)**

**logic2 i1 (**

**// port map - connection between master ports and signals/registers**

**.a0(a0),**

**.a1(a1),**

**.a2(a2),**

**.a3(a3),**

**.a4(a4),**

**.a5(a5),**

**.a6(a6),**

**.a7(a7),**

**.dout0(dout0),**

**.dout1(dout1),**

**.dout2(dout2),**

**.enb(enb)**

**);**

**initial**

**begin**

**// code that executes only once**

**// insert code here --> begin**

**enb = 0;**

**a0 = 0 ;**

**a1 = 0 ;**

**a2 = 0 ;**

**a3 = 0 ;**

**a4 = 0 ;**

**a5 = 0 ;**

**a6 = 0 ;**

**a7 = 0 ;**

**#50**

**a7=1;**

**a6=0;**

**#10**

**a6 = 1 ;**

**a5 = 1 ;**

**a4 = 0 ;**

**#30**

**a6 = 1 ;**

**a5 = 1 ;**

**a4 = 1 ;**

**a3 = 1 ;**

**a2 = 1 ;**

**a1 = 0 ;**

**# 40**

**enb = 1;**

**#20**

**enb = 0;**

**a0 = 1 ;**

**a1 = 1 ;**

**a2 = 1 ;**

**a3 = 1 ;**

**a4 = 1 ;**

**a5 = 1 ;**

**a6 = 1 ;**

**a7 = 1 ;**

**// --> end**

**$display("Running testbench");**

**end**

**endmodule**

（2）3线-8线译码器

// Copyright (C) 2018 Intel Corporation. All rights reserved.

// Your use of Intel Corporation's design tools, logic functions

// and other software and tools, and its AMPP partner logic

// functions, and any output files from any of the foregoing

// (including device programming or simulation files), and any

// associated documentation or information are expressly subject

// to the terms and conditions of the Intel Program License

// Subscription Agreement, the Intel Quartus Prime License Agreement,

// the Intel FPGA IP License Agreement, or other applicable license

// agreement, including, without limitation, that your use is for

// the sole purpose of programming logic devices manufactured by

// Intel and sold by Intel or its authorized distributors. Please

// refer to the applicable agreement for further details.

// \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// This file contains a Verilog test bench template that is freely editable to

// suit user's needs .Comments are provided in each section to help the user

// fill out necessary details.

// \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Generated on "03/12/2020 11:17:19"

// Verilog Test Bench template for design : a74HC138

//

// Simulation tool : ModelSim-Altera (Verilog)

//

**`timescale 1 ns/ 1 ps**

**module a74HC138\_vlg\_tst();**

**// constants**

**// general purpose registers**

**//reg eachvec;**

**// test vector input registers**

**reg a0;**

**reg a1;**

**reg a2;**

**reg enb;**

**// wires**

**wire dout0;**

**wire dout1;**

**wire dout2;**

**wire dout3;**

**wire dout4;**

**wire dout5;**

**wire dout6;**

**wire dout7;**

**// assign statements (if any)**

**a74HC138 i1 (**

**// port map - connection between master ports and signals/registers**

**.a0(a0),**

**.a1(a1),**

**.a2(a2),**

**.dout0(dout0),**

**.dout1(dout1),**

**.dout2(dout2),**

**.dout3(dout3),**

**.dout4(dout4),**

**.dout5(dout5),**

**.dout6(dout6),**

**.dout7(dout7),**

**.enb(enb)**

**);**

**initial**

**begin**

**// code that executes only once**

**// insert code here --> begin**

**enb = 0;**

**a0 = 0 ;**

**a1 = 0 ;**

**a2 = 0 ;**

**#50**

**a1=1;**

**a2=0;**

**#10**

**a2 = 1 ;**

**a0 = 1 ;**

**a1 = 0 ;**

**#30**

**a2 = 1 ;**

**a1 = 0 ;**

**# 40**

**enb = 1;**

**#20**

**enb = 0;**

**a0 = 1 ;**

**a1 = 1 ;**

**a2 = 1 ;**

**// --> end**

**$display("Running testbench");**

**end**

**endmodule**

（3）显示译码器

// Copyright (C) 2018 Intel Corporation. All rights reserved.

// Your use of Intel Corporation's design tools, logic functions

// and other software and tools, and its AMPP partner logic

// functions, and any output files from any of the foregoing

// (including device programming or simulation files), and any

// associated documentation or information are expressly subject

// to the terms and conditions of the Intel Program License

// Subscription Agreement, the Intel Quartus Prime License Agreement,

// the Intel FPGA IP License Agreement, or other applicable license

// agreement, including, without limitation, that your use is for

// the sole purpose of programming logic devices manufactured by

// Intel and sold by Intel or its authorized distributors. Please

// refer to the applicable agreement for further details.

// \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// This file contains a Verilog test bench template that is freely editable to

// suit user's needs .Comments are provided in each section to help the user

// fill out necessary details.

// \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Generated on "03/13/2020 10:27:07"

// Verilog Test Bench template for design : a7448

//

// Simulation tool : ModelSim-Altera (Verilog)

//

**`timescale 1 ns/ 1 ps**

**module a7448\_vlg\_tst();**

**// constants**

**// general purpose registers**

**//reg eachvec;**

**// test vector input registers**

**reg a0;**

**reg a1;**

**reg a2;**

**reg a3;**

**reg enb;**

**// wires**

**wire dout0;**

**wire dout1;**

**wire dout2;**

**wire dout3;**

**wire dout4;**

**wire dout5;**

**wire dout6;**

**// assign statements (if any)**

**a7448 i1 (**

**// port map - connection between master ports and signals/registers**

**.a0(a0),**

**.a1(a1),**

**.a2(a2),**

**.a3(a3),**

**.dout0(dout0),**

**.dout1(dout1),**

**.dout2(dout2),**

**.dout3(dout3),**

**.dout4(dout4),**

**.dout5(dout5),**

**.dout6(dout6),**

**.enb(enb)**

**);**

**initial**

**begin**

**// code that executes only once**

**// insert code here --> begin**

**enb = 0;**

**a0 = 0 ;**

**a1 = 0 ;**

**a2 = 0 ;**

**a3 = 0 ;**

**#100**

**a1=1;**

**a0=0;**

**#100**

**a0 = 1 ;**

**a1 = 1 ;**

**a2 = 0 ;**

**#100**

**a3 = 1 ;**

**a2 = 0 ;**

**a1 = 0 ;**

**#100**

**enb = 1;**

**#100**

**a3 = 0 ;**

**a2 = 1 ;**

**a1 = 0 ;**

**#100**

**enb = 0;**

**a0 = 1 ;**

**a1 = 1 ;**

**a2 = 1 ;**

**a3 = 1 ;**

**// --> end**

**$display("Running testbench");**

**end**

**endmodule**

（4）多路选择器

// Copyright (C) 2018 Intel Corporation. All rights reserved.

// Your use of Intel Corporation's design tools, logic functions

// and other software and tools, and its AMPP partner logic

// functions, and any output files from any of the foregoing

// (including device programming or simulation files), and any

// associated documentation or information are expressly subject

// to the terms and conditions of the Intel Program License

// Subscription Agreement, the Intel Quartus Prime License Agreement,

// the Intel FPGA IP License Agreement, or other applicable license

// agreement, including, without limitation, that your use is for

// the sole purpose of programming logic devices manufactured by

// Intel and sold by Intel or its authorized distributors. Please

// refer to the applicable agreement for further details.

// \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// This file contains a Verilog test bench template that is freely editable to

// suit user's needs .Comments are provided in each section to help the user

// fill out necessary details.

// \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Generated on "03/06/2020 11:50:21"

// Verilog Test Bench template for design : mux41\_a

//

// Simulation tool : ModelSim-Altera (Verilog)

//

**`timescale 1 ns/ 1 ps**

**module mux41\_a\_vlg\_tst();**

**// constants**

**// general purpose registers**

**//reg eachvec;**

**// test vector input registers**

**reg a0;**

**reg a1;**

**reg a2;**

**reg a3;**

**reg s0;**

**reg s1;**

**// wires**

**wire y;**

**// assign statements (if any)**

**mux41\_a i1 (**

**// port map - connection between master ports and signals/registers**

**.a0(a0),**

**.a1(a1),**

**.a2(a2),**

**.a3(a3),**

**.s0(s0),**

**.s1(s1),**

**.y(y)**

**);**

**initial**

**begin**

**a0=2'b00;**

**a1=2'b01;**

**a2=2'b10;**

**a3=2'b11;**

**s1=1'b0;s0=1'b0;**

**#100**

**s1=1'b0;s0=1'b1;**

**#100**

**s1=1'b1;s0=1'b0;**

**#100**

**s1=1'b1;s0=1'b1;**

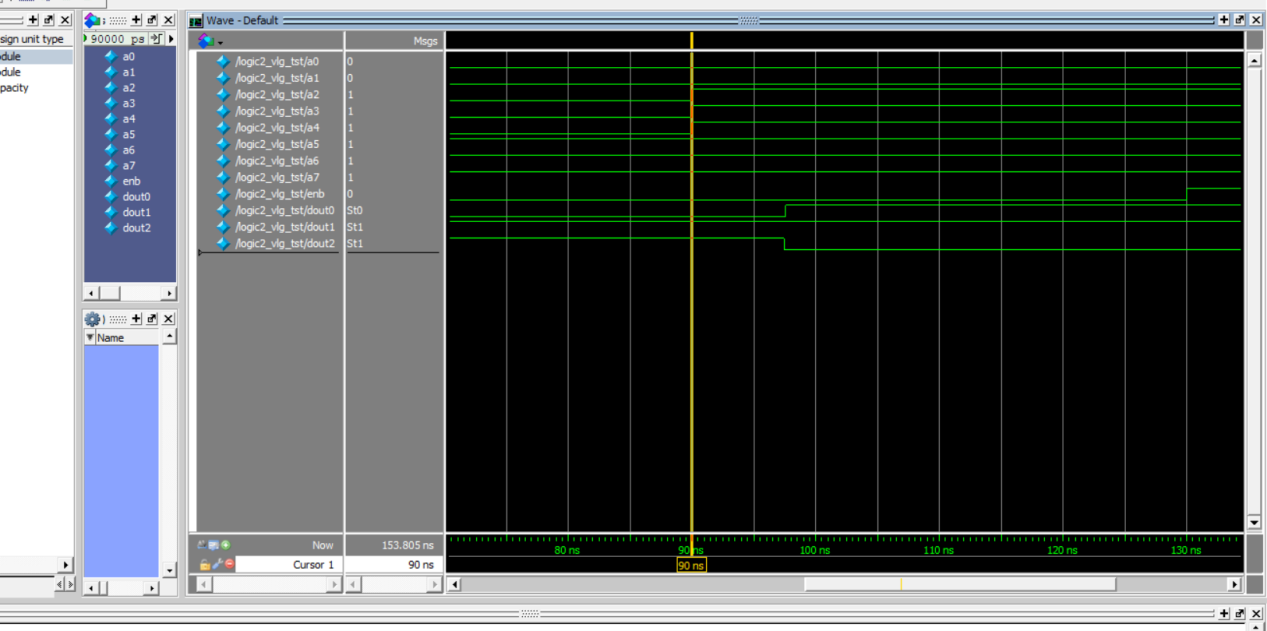
**#100;**

**end**

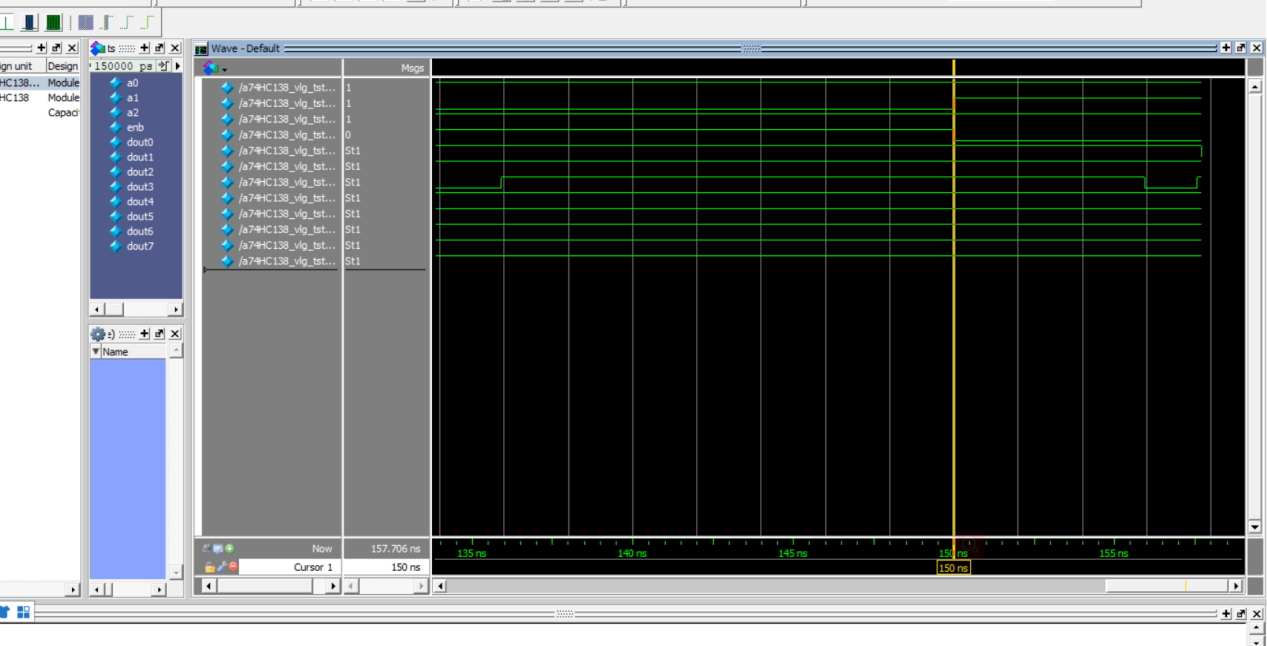
**endmodule**

1. Quartus仿真效果图

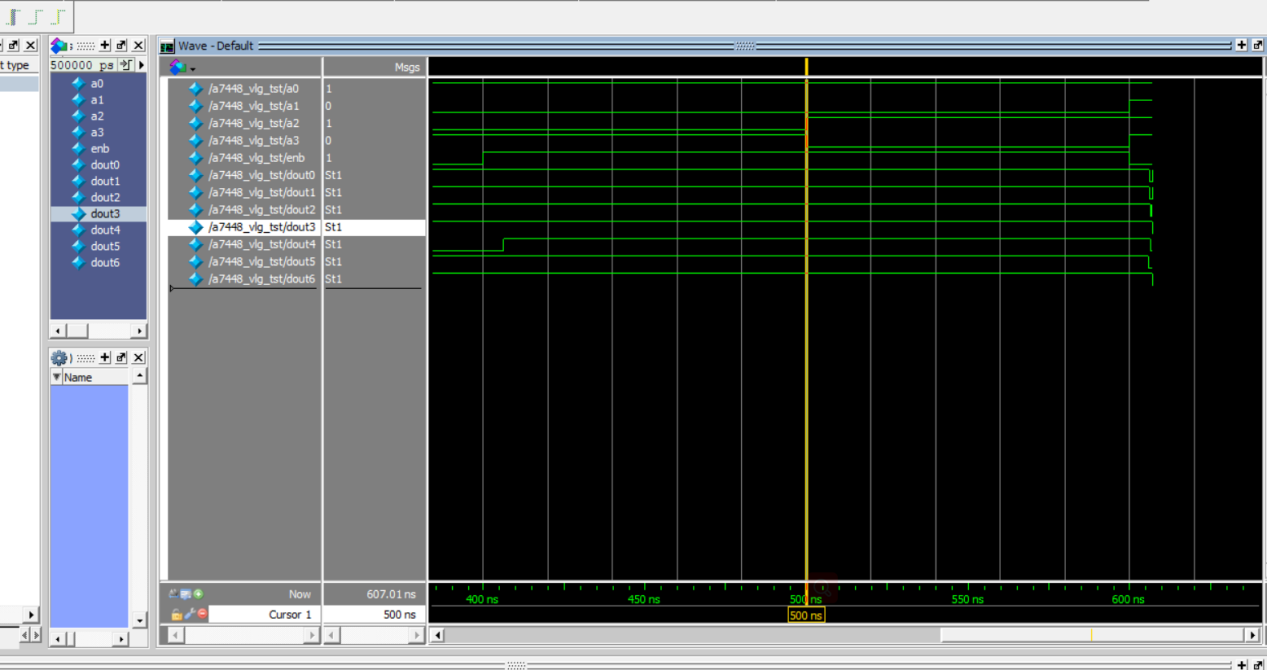
（1）8线-3线优先编码器



（2）3线-8线译码器



（3）显示译码器



（4）多路选择器

